WHAT IS CLAIMED IS:

1. A semiconductor device comprising a tristate buffer circuit including, on an output stage, at least a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state, said semiconductor device further comprising

a control circuit performing control for speeding up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state.

2. The semiconductor device as defined in claim 1, wherein said control circuit includes a circuit which, when said control signal is of a value indicating the enable state, and a signal determining the on/off of said first transistor is of a level indicating the on-state of said first transistor, performs control to shorten the time until said signal determining the on/off of said first transistor gets to a level of turning off said first transistor at the time of switching of said control signal from said enable state to said disable state.

3. The semiconductor device as defined in claim 1, further comprising:

a logic circuit for receiving said data signal and said control signal as inputs and outputting a first signal for controlling the on/off of said first transistor; and

a transmission gate including a third transistor being turned on when said control signal is of a value indicating the enable state and receiving said first signal output from said logic circuit to transfer said first signal to a control terminal of said first transistor, said third transistor being turned off when said control signal is of the value indicating the disable state; wherein

said control circuit includes a circuit for receiving said control signal and delaying the timing of changing over the state of said third transistor of said transmission gate from an on-state to an off-state at the time of switching the state of said control signal from the enable state to the disable state; and wherein

during the time said third transistor is on, when the state of said control signal is switched from the enable state to the disable state, said transmission gate transfers the level of said first signal output from said logic circuit for turning off said first transistor to a control terminal of said first transistor to speed up the transition from the on-state to the off-state of said first transistor.

4. The semiconductor device as defined in claim 1, wherein said control circuit includes a circuit for rendering a path across the control terminal of said first transistor and the power supply electrically conductive responsive to said control signal to set the control terminal of said first transistor to a voltage which turns off said first transistor.

5. The semiconductor device as defined in claim 1, further comprising:

a first logic circuit for receiving said data signal and said control

signal as inputs and outputting a first signal controlling the on/off of said first transistor; and

a transmission gate connected across an output terminal of said first logic circuit and the control terminal of said first transistor;

wherein said first logic circuit outputs a second logic value as said first signal, when said control signal indicates the enable state and said data signal is of a first logic value, and outputs the first logic value, as said first signal, without dependency on the value of said data signal, when said control signal is of a value indicating the disable state;

wherein said first transistor is turned on and off when the control terminal of said first transistor is of the second logic value and of the first logic value, respectively;

wherein said transmission gate includes a third transistor controlled to be on when said control signal is in the enable state;

wherein said control circuit includes a timing adjustment circuit for receiving said control signal and delaying the transition timing from the enable state to the disabled state of said control signal to output the delayed signal as a second control signal; and

wherein said third transistor of said transmission gate is changed over from an on-state to an off-state based on transition from the enable state to the disable state of said second control signal output from said timing adjustment circuit.

6. The semiconductor device as defined in claim 5, wherein said timing adjustment circuit includes a delay circuit for receiving and delaying said control signal a preset time to output the delayed signal.

7. The semiconductor device as defined in claim 5, wherein said timing adjustment circuit includes

a delay circuit for receiving said control signal and delaying the signal a preset time to output the delayed signal; and

a logic circuit for receiving said control signal and an output signal of said delay circuit and delaying a preset time the transition from the enable state to the disable state of said control signal to output the delayed signal as said second control signal.

8. The semiconductor device as defined in claim 1, further comprising:

a first logic circuit for receiving said data signal and said control signal as inputs and outputting a first signal controlling the on/off of said first transistor; and

a transmission gate connected across an output terminal of said first logic circuit and the control terminal of said first transistor;

wherein said first logic circuit outputs a second logic value as said first signal, when said control signal indicates the enable state and said data signal is of a first logic value, and outputs the first logic value, as said first signal, without dependency on the value of said data signal, when said control signal is of a value indicating the disable state;

wherein said first transistor is turned on and off when the control terminal of said first transistor is of the second logic value and of the first logic value, respectively;

wherein said transmission gate includes a third transistor controlled to be on when said control signal is in the enable state;

wherein said control circuit includes a circuit connected across the control terminal of said first transistor and the power supply, said circuit, when said control signal is of a value indicating the enable state, rendering a path between said power supply and a control terminal node of said first transistor to an electrically non-conductive state; said circuit, when said control signal is of a value indicating the disable state, rendering the path between said power supply and a control terminal node of said first transistor to an electrically conductive state to set the voltage of the control terminal of said first transistor to a level of turning off said first transistor.

9. The semiconductor device as defined in claim 5, wherein said control circuit further includes a circuit connected across the control terminal of said first transistor and the power supply;

wherein said circuit, when said control signal is of a value indicating the enable state, renders a path between said power supply and a control terminal node of said first transistor to an electrically non-conductive state; and

wherein said circuit, when said control signal is of a value indicating the disable state, renders the path between said power supply and a control terminal node of said first transistor to an electrically conductive state to set the voltage of the control terminal of said first transistor to a level of turning off said first transistor.

10. The semiconductor device as defined in claim 1, further comprising:

a second logic circuit for receiving said control signal and said

data signal as inputs and outputting a second signal controlling the on/off of said second transistor; an output terminal of said second logic circuit being connected to a control circuit of said second transistor;

wherein said second logic circuit, when said control signal indicates an enable state and said data signal assumes first and second logic values, outputs, as said second signal, an output signal causing said second transistor to be turned off and on; and

wherein said second logic circuit, when said control signal indicates a disable state, outputs an output signal causing said second transistor to be turned off, as said second signal, without dependency on said data signal.

11. The semiconductor device as defined in claim1, further comprising:

a pad connected to an output node of said first transistor and composing an output of said tristate buffer circuit; and

a bypass circuit connected across the control terminal of said first transistor and an output node of said first transistor for forming a bypass across the output node of said first transistor and said control terminal of said first transistor, when the voltage applied to said pad is equal to or higher than the power supply voltage of said tristate buffer.

12. The semiconductor device as defined in claim 5, further comprising:

a pad composing an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential and composing said transmission gate, said

fourth transistor being of the conductivity type (termed a 'second conductivity type') opposite to the conductivity type of said third transistor (termed a 'first conductivity type') which is turned on when said second control signal from said timing adjustment circuit is of a value indicating the enable state;

a series circuit including a fifth transistor of the second conductivity type, having a control gate supplied with the power supply potential and a sixth transistor of the second conductivity type, controlled to an off-state and to an on-state when said second control signal from said timing adjustment circuit is of a value indicating the enable state and of a value indicating the disable state, respectively, said series circuit connected between the control terminal of said third transistor and said pad; and

a seventh transistor of the first conductivity type having a control terminal supplied with the power supply potential, between the control terminal of said third transistor and said pad, in parallel with said series circuit.

13. The semiconductor device as defined in claim 5, further comprising:

a pad composing an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential, and composing said transmission gate, said fourth transistor being of the conductivity type (termed a 'second conductivity type') opposite to the conductivity type of said third transistor (termed a 'first conductivity type') which is turned on when

said second control signal from said timing adjustment circuit is of a value indicating the enable state;

a fifth transistor of the second conductivity type, between the control terminal of said third transistor and said pad, said fifth transistor being controlled to be off and on when said second control signal from said timing adjustment circuit is of a value indicating the enable state and the disable state, respectively;

a sixth transistor of the first conductivity type having a control terminal supplied with the power supply potential and connected between the control terminal of said third transistor and said pad, in parallel with said fifth transistor.

14. The semiconductor device as defined in claim 8, further comprising:

a pad composing an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential, and composing said transmission gate, said fourth transistor being of the conductivity type (termed a 'second conductivity type') opposite to the conductivity type of said third transistor (termed a 'first conductivity type') which is turned on when said second control signal from said timing adjustment circuit is of a value indicating the enable state;

a series circuit including a fifth transistor of the second conductivity type, having a control gate supplied with the power supply potential and a sixth transistor of the second conductivity type, controlled to an off-state and to an on-state when said second control

signal from said timing adjustment circuit is of a value indicating the enable state and of a value indicating the disable state, respectively, said series circuit connected between the control terminal of said third transistor and said pad; and

a seventh transistor of the first conductivity type having a control terminal supplied with the power supply potential, between the control terminal of said third transistor and said pad, in parallel with said series circuit.

15. The semiconductor device as defined in claim 8, further comprising:

a pad composing an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential, and composing said transmission gate, said fourth transistor being of the conductivity type (termed a 'second conductivity type') opposite to the conductivity type of said third transistor (termed a 'first conductivity type') which is turned on when said second control signal from said timing adjustment circuit is of a value indicating the enable state;

a fifth transistor of the second conductivity type, between the control terminal of said third transistor and said pad, said fifth transistor being controlled to be off and on when said second control signal from said timing adjustment circuit is of a value indicating the enable state and the disable state, respectively;

a sixth transistor of the first conductivity type having a control terminal supplied with the power supply potential and connected

between the control terminal of said third transistor and said pad, in parallel with said fifth transistor.

16. The semiconductor device as defined in claim 1, further comprising:

a pad connected to an output node of said first transistor and composing an output of said tristate buffer circuit; and

an eighth transistor provided in a well region common to the well region of said first transistor or in a well region connected to the well region of said first transistor, said eighth transistor being of the same conductivity type as said first transistor and having a control terminal connected to said pad;

wherein electric connection between said well region and the power supply is controlled to be in an off-state through said eighth transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

17. The semiconductor device as defined in claim 5, further comprising:

a pad connected to an output node of said first transistor and composing an output of said tristate buffer circuit; and

an eighth transistor provided in a well region common to the well region of said first transistor or in a well region connected to the well region of said first transistor, said eighth transistor having a control terminal connected to said pad and being of the same conductivity type as said first transistor;

wherein the third transistor composing said transmission gate is

arranged in a well region common to a well region of said first transistor and/or said eighth transistor or in a well region connected to the well regions of said first transistor and said eighth transistor; and

wherein electric connection between said well region associated with said first, third and eighth transistors and the power supply are controlled to be in an off-state through said eighth transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

18. The semiconductor device as defined in claim 16, further comprising

a ninth transistor of the same conductivity type as said first transistor, having the control terminal supplied with the power supply potential and connected across the control terminal and an output node of said first transistor; said ninth transistor being provided in a well region common to the well region of said first transistor and/or said eighth transistor or in a well region connected to the well region of said first transistor and said eighth transistor; wherein electric connection between said well region associated with said ninth transistor and the power supply is controlled to be in an off-state through said eighth transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

19. The semiconductor device as defined in claim 5, further comprising

a tenth transistor between the control terminal of said third transistor of said transmission gate and a second power supply, said

tenth transistor having a control terminal supplied with said second control signal output from said timing adjustment circuit and being turned on and off when said second control signal is of a value indicating the enable state and the disable state, respectively.

20. The semiconductor device as defined in claim 8, further comprising

a tenth transistor between the control terminal of said third transistor of said transmission gate and a second power supply, said tenth transistor having a control terminal supplied with said control signal and being turned on and off when said control signal is of a value indicating the enable state and the disable state, respectively.

21. The semiconductor device as defined in claim 19, further comprising

an eleventh transistor connected across the control terminal of said third transistor of said transmission gate and an output node of said tenth transistor and having a control terminal supplied with the power supply potential.

22. The semiconductor device as defined in claim 1, further comprising

a twelfth transistor between a pad composing an output of said tristate buffer circuit and an output of said second transistor, and having a control terminal supplied with the power supply potential.

23. The semiconductor device as defined in claim 3, further comprising:

a pad composing an output of said tristate buffer circuit; wherein

said control circuit including a circuit receiving a signal reflecting the voltage of said pad and said control signal to perform control to cause said third transistor composing said transmission gate, to be transiently turned on, during transition from said enable state to the disable state of said control signal, when said signal reflecting the pad voltage indicates a high level voltage.

24. The semiconductor device as defined in claim 5, further comprising

a one-shot pulse generating circuit for receiving said control signal and detecting the switching from the enable state to the disable state of said control signal to generate a one-shot pulse signal of a preset pulse width; and

a thirteenth transistor connected across an output node of said tristate buffer circuit and a second power supply for receiving an output signal of said one-shot pulse generating circuit, said thirteenth transistor being turned on during the period as determined by the pulse width of said one-shot pulse signal.

25. The semiconductor device as defined in claim 1, further comprising:

a one-shot pulse generating circuit for receiving said control signal and detecting the switching from the enable state to the disable state of said control signal to generate a one-shot pulse signal of a preset pulse width; and

a logic circuit for receiving said data signal and an output signal of said one-shot pulse generating circuit to generate a signal which turns

on said second transistor when said data signal is of the second logic value or when said one-shot pulse signal is active.

26. The semiconductor device as defined in claim 8, wherein said control circuit includes at least two transistors connected in series across the control terminal of said first transistor and said power supply;

one of said two transistors being connected in a diode configuration;

the other transistor having a control terminal supplied with said control signal and being turned off and on when said control signal is of a value indicating the enable state and the disable state, respectively.

27. The semiconductor device as defined in claim 26, further comprising

a pad connected to an output of said tristate buffer circuit;

wherein one of said transistors of said control circuit is provided in a well region common to the well region of said first transistor and/or the well region of said eighth transistor or in said well regions of said first transistor and said eighth transistor; and wherein electric connection between the power supply and said well regions of said first and third transistors and the one transistor of said control circuit is controlled to be in an off-state through said eighth transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

28. The semiconductor device as defined in claim 1, wherein said tristate buffer circuit is a tolerant buffer circuit capable of applying in a disable state a voltage higher than the power supply voltage of said

tristate buffer circuit or than said driving power supply voltage.

29. The semiconductor device as defined in claim 1, further comprising an I/O buffer circuit including:

a pad connected to an output of said tristate buffer circuit; and

an input buffer connected to said pad;

wherein said tristate buffer circuit, said pad and said input buffer compose an I/O buffer circuit which is set to an output mode of outputting a level corresponding to said data signal from said tristate buffer circuit to said pad when said control signal is of a value indicating the enable state; and

wherein said I/O buffer circuit is set to an input mode of receiving a signal applied to said pad by said input buffer when said control signal is of a value indicating the disable state.

30. The semiconductor device as defined in claim 29, further comprising

a circuit connected across said pad and said input buffer for supplying a signal of the level of said power supply voltage to an input end of the input buffer when the voltage equal to or higher than the power supply voltage of said tristate buffer is applied to said pad.

31. The semiconductor device as defined in claim 5, further comprising:

a pad composing an output of said tristate buffer circuit; wherein

said timing adjustment circuit receives a signal reflecting the voltage of said pad and said control signal to perform control to cause said third transistor composing said transmission gate to be transiently

turned on, during transition from said enable state to the disable state of said control signal, when said signal reflecting the pad voltage indicates a high level voltage.

32. The semiconductor device as defined in claim 8, further comprising:

a pad composing an output of said tristate buffer circuit; wherein said control circuit include a circuit receiving a signal reflecting the voltage of said pad and said control signal to perform control to cause said third transistor composing said transmission gate to be transiently turned on, during transition from said enable state to the disable state of said control signal, when said signal reflecting the pad voltage indicates a high level voltage.

33. The semiconductor device as defined in claim 9, wherein said control circuit includes at least two transistors connected in series across the control terminal of said first transistor and said power supply;

one of said two transistors being connected in a diode configuration;

the other transistor having a control terminal supplied with said control signal and being turned off and on when said control signal is of a value indicating the enable state and the disable state, respectively.